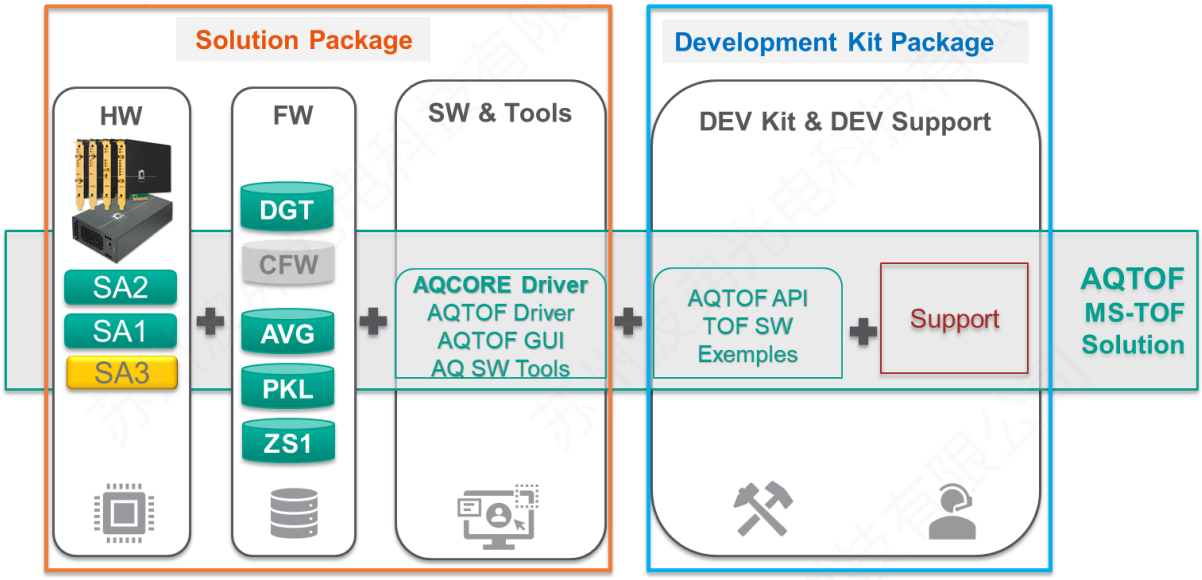
Geneva, Switzerland, 2023

Acqiris AQTOF Solution Description

Acqiris AQTOF Solution is primarily aimed at addressing the specific data acquisition and data processing capabilities required for TOFMS (Time-of-Flight Mass Spectrometry) applications. It can also be used efficiently in many time-domain pulse-analysis applications.

Acqiris AQTOF Solution is split into two separate packages that specifically targets the different design, development, qualification and the manufacturing phase of your instrument life cycle. The AQTOF Solution package is a bundle composed of a DAQ module, a set of applicative FWs, the SW device drivers and some SW tools required to install, operate, and maintain the AQTOF solution within your instrument. The AQTOF Development Kit is aimed to enable the smooth and efficient integration of the AQTOF solution within your application framework. It contains all the required SW components, programming examples, SW tools and allocated support for integrating and qualifying the AQTOF solution into your specific system environment.

Figure 1 shows the high-level AQTOF solution segmentation and associated deliverables.

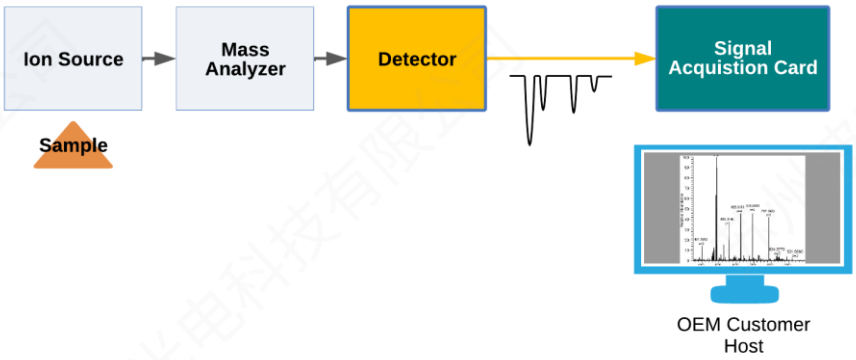


Time-of-Flight Mass Spectrometry (TOFMS) Instrument

Mass spectrometry is an analysis technique used to detect, identify, and quantify molecules of interest by measuring their mass, and to characterize their chemical structure.

While mass spectrometry systems now come in numerous configurations, their performance largely depends on a few fundamental elements. Therefore, a mass spectrometer can be broken down into three main components. The heart of the device is the ion source which creates from the samples material the ions to be identified. The ions are then passed along to one or several different mass analyzers, allowing them to be separated according to their mass and charge. Finally, the individual ions are passed down a vacuum tube, at the end of which is a detector that senses the charged ions and displays the results as an ion spectrum. Acqiris DAQ module products precisely measure the time for ions to reach the detector at a resolution of few picoseconds and provide onboard application pre-processing capabilities to improve the complex measurements duty-cycle.

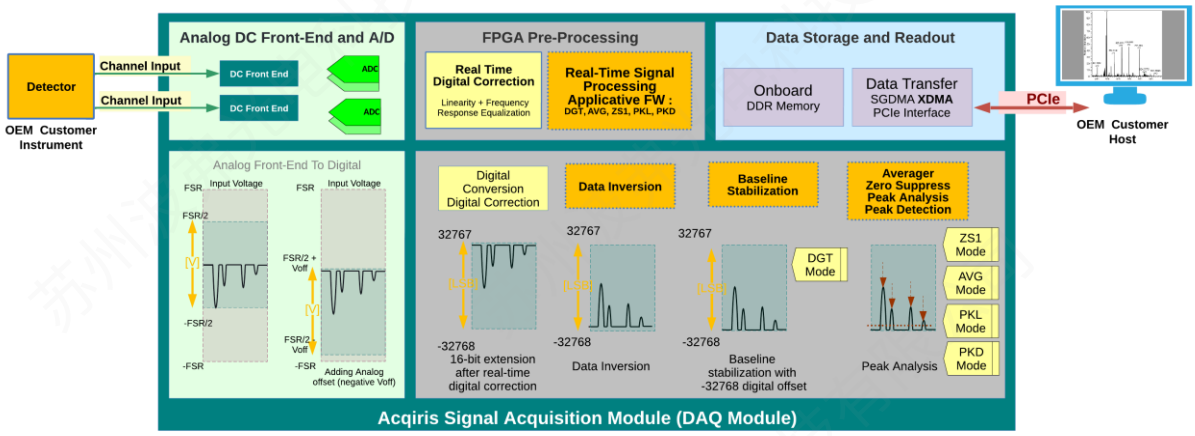
Figure 2 presents a simplified block diagram of the main parts of a TOFMS instrument.



AQTOF Solution

Acqiris AQTOF Solution provides a complete application solution addressing the different needs of your detector pulse characteristics and your system measurement and duty-cycle requirements.

Figure 3 presents the typical data flow diagram used in a TOFMS application from the analog input fed by the detector output signal to the digital sample representation in the host machine.



Signal Acquisition and processing data flow

Acqiris DAQ modules are designed to provide unique signal fidelity and especially low-noise DC front-end using dedicated IC technology and patented front-end circuitry. While using unipolar input pulse waveform as provided by ion detector, it is possible to take advantage of the DC offset capability to shift the observable data window to place the input baseline close to FSR/2 by adding a negative analog offset on the input signal. Then Acqiris front-end amplifier provides to each interleaved ADC cores the amplified input analog signal that is digitally converted and transmitted to the onboard FPGA. A digital correction block can be used to compensate the ADC core's non-linearity and interleave mismatches based on a board manufacturing characterization. It results in a digital signed data format extension compared to the original ADC raw samples value. An optional frequency equalization profile can also be applied to improve the frequency response of the DAQ module.

The pre-processed data are then passed to the applicative firmware part which contains both the data inversion and baseline stabilization capability before being ready to be further analyzed or simply offloaded to the host application through the efficient PCIe interface.

Acqiris AQTOF solution is providing several FPGA onboard pre-processing modes to offload the processing and analyzing tasks from the host that will be further described in the next section.

AQTOF Solution Features

Digital Linearity Correction

Acqiris DC front-end technology ensures low-noise and low distortion acquisition of your analog signal with a specific emphasis on correcting any non-linearity sources that can affect the relative peak intensity versus compounds concentration. For high-resolution DAQ modules a specific manufacturing characterization is carried out to optimize the linearity response of the complete analog chain.

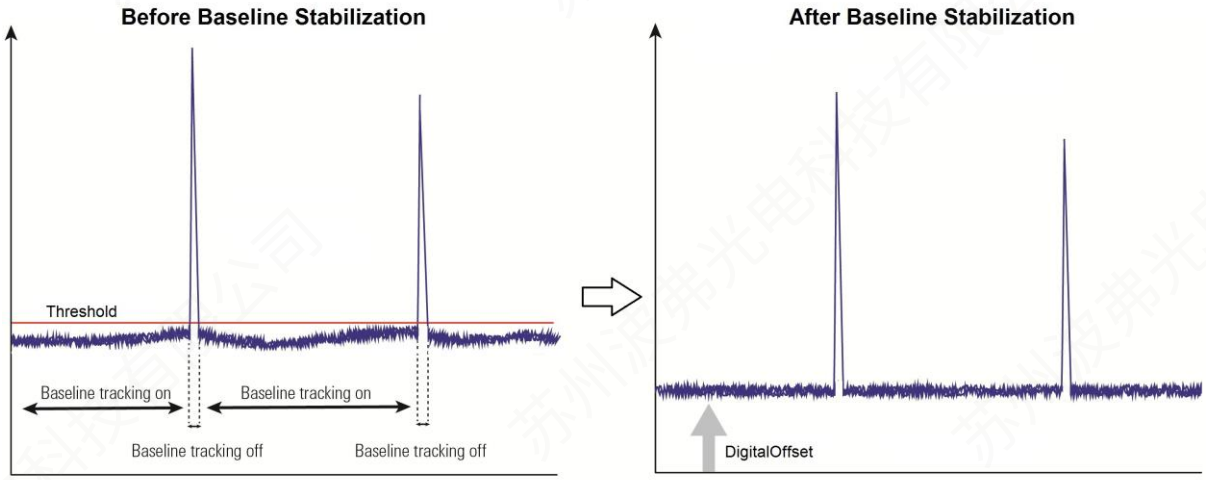
Calibration at Target Voltage

The Calibration at target voltage feature is a calibration optimization used to minimize the apparent noise of the baseline. The baseline is commonly placed at the near end of the observable data window where any gain and offset errors are magnified. In interleaved ADC configurations those errors create an apparent pattern noise that impacts the achievable dynamic range.

Baseline Stabilization

The use of the baseline stabilization feature is recommended for time-domain applications that need a very stable signal input baseline and are using a high resolution DAQ module. The baseline fluctuation can result from various factors including the DAQ module sensitiveness to low frequency noise (usually referred as 1/f noise in ADC) or from the consequences of the system noise and drift on the input signal driven by the detector.

The baseline stabilization is carried out with a configurable baseline estimator engine that is tracking and removing the estimated baseline. A digital offset can then be applied to restore the original theoretical baseline.



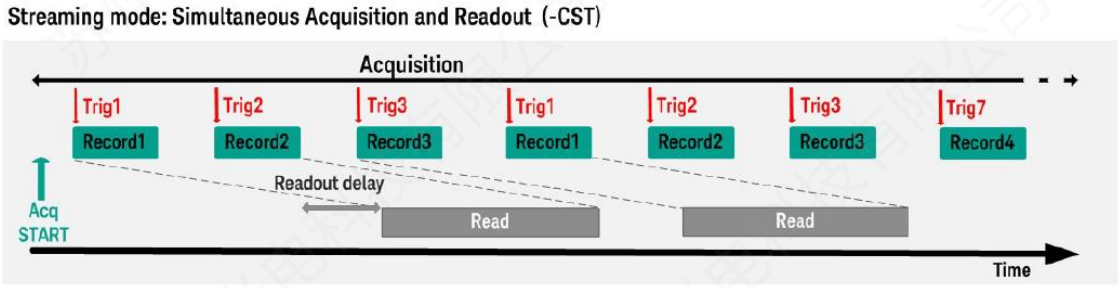
Digital Equalization Profiles

The digital equalization feature is aimed to improve the frequency response of the SA2 product family and compensates for signal distortion resulting from the large analog front-end bandwidth. By default, the digital frequency equalization is disabled, and two equalization profiles can be selected: The *smooth roll-off* profile that minimizes the pulse overshoot and ringing, the *sharp roll-off* that optimizes the frequency response flatness.

Customized frequency equalization profile can also be developed on demand as an AQTOF solution option.

Simultaneous Acquisition and Readout (*CST readout Mode*)

The Simultaneous Acquisition and Readout streaming mode (CST) provides the capability for simultaneous DAQ module acquisition and data readout with triggered acquisitions. Compared with standard acquisition mode, this readout mode enables lower latency, longer acquisition duration, and is dedicated to applications requiring no trigger loss.



Decimated sampling rate with associated low pass filters (*Available in both DGT and AVG Mode*)

The decimated sampling rate feature provides a programmable binary decimation of the sampling rate associated with an alias protection. It can be used to safely lower the sampling rate to address longer flight time acquisition need with a coarser time resolution. The optional anti-aliasing low-pass filters contribute to a SNR improvement by lowering the broadband noise contribution.

Programmable Self-Trigger (*Available in both DGT and AVG Mode*)

The Self-Trigger feature provides a programmable and autonomous internal trigger signal generation that is output on the front-panel TRG OUT connector and can be used to trigger your instrument. This configurable trigger source is synchronous to the ADC sampling clock and is aimed to minimize both the system jitter while accumulating multiple data records and the contribution of the DAQ module synchronous noise.

Synchronized Serial Output

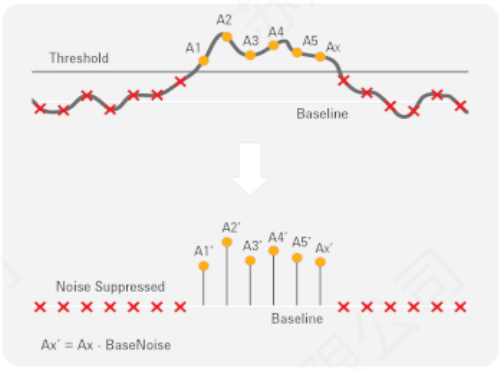
The Synchronized serial output provides up to three programmable LVTTL control signals that are synchronous to the ADC sampling clock. Each Synchronized output can be defined as an independent configurable pulse generator to provide a tight control of your instrument minimizing the overall system jitter.

Real-time sampling and averaging mode (*AVG Mode*)

The real-time sampling and averaging mode can be used to improve the signal-to-noise ratio of repetitive input signal by lowering the random noise contribution. The averaging is performed in real-time by accumulating successive recorded waveforms into an "accumulated record" which is provided for the readout. It also enables to reduce the amount of data to be transferred while strengthening the intensity of low abundance compounds. Depending on the HW capabilities, the number of accumulations can be up to 512K and accumulated record length up to 1M points[1].

Noise Suppress Accumulation (*Available in AVG Mode*)

The Noise Suppress Accumulation feature is a thresholding capability aimed to identify rare peak events sitting on top of a noisy baseline. To enhance the DAQ module ability to detect such signals in the presence of synchronous noise, the real-time sampling and averaging mode allows the user to set a programmable threshold that must be exceeded for each data value to be considered in the accumulation process.

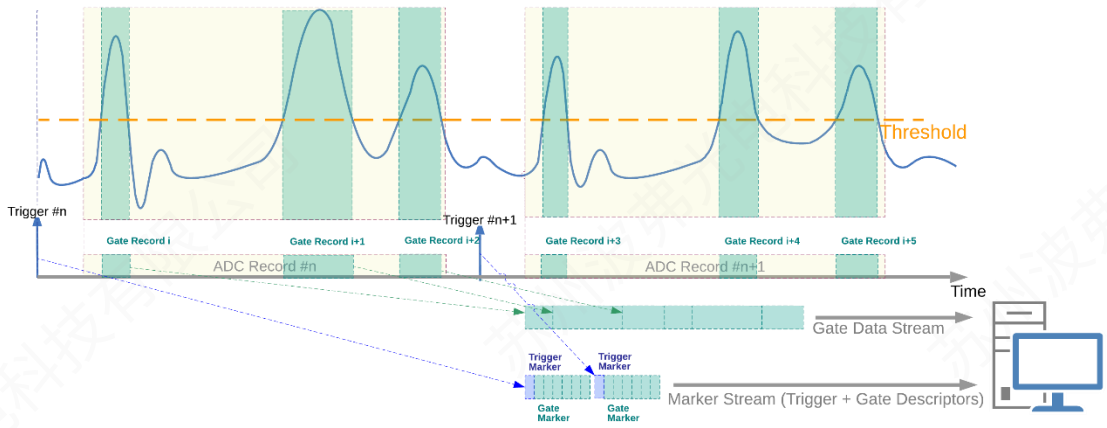


Partial averaging mode (PKL Mode)

This feature is providing a limited accumulation capability in the FPGA FW while keeping the same sample size as the original corrected ADC Sample one. It can be combined with a SW accumulation at the application level to provide a similar capability as the standard AVG mode but while also supporting the PKL capability.

Zero-Suppress mode (*ZS Mode*)

The zero-suppress mode is a data reduction mode allowing to gate the data acquisition above a user-defined threshold, as depicted on figure below. The threshold allows to identify the signal of interest.



[1] Larger number of accumulations are also possible considering a combined FW+SW accumulation scheme.

This feature allows data compression: signal data not complying with user criteria are suppressed and only the data complying with user criteria are stored and transferred as 'gated' data to host computer along with trigger and gate timestamp information that enables to reconstruct the original waveform.

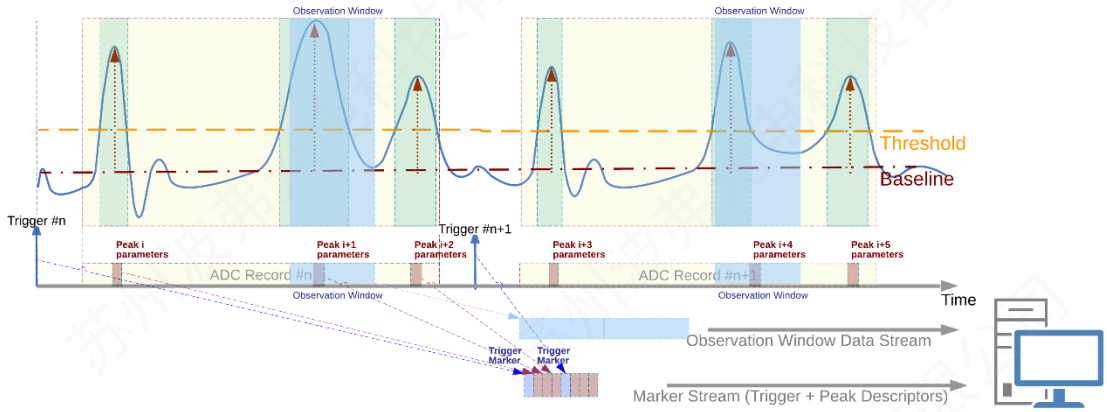
Peak List Mode (*PKL Mode*)

The real-time peak-listing is a dedicated acquisition mode (PKL) intended to address time-domain pulse applications analysis. It performs a real-time analysis of the raw data to identify signal peaks according to user-programmable pulse identification criteria and then list and extract their key characteristics. The pulse parameters such as the peak position, peak intensity, center of mass and peak area can be automatically extracted and directly transferred to the host application.

The acquisition and analysis of a signal record can be performed while reading the result of the previous record, minimizing the dead time between successive record analysis.

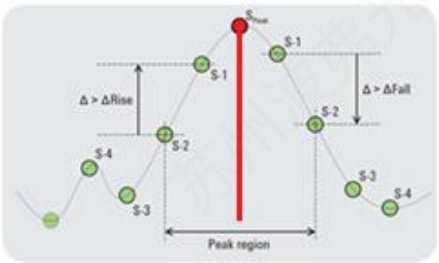
Observation Window (*PKL Mode*)

The observation window capability provides in parallel to the PKL metadata stream the capability to also return the raw data used for the peak analysis. It enables not only to correlate the automatic firmware peak parameters extraction but also let the user define complementary peak identification capability for unresolved peak spectrum.



Peak Detection mode (PKD Mode)

The peak detection mode is a dedicated acquisition mode (PKD) intended to address time-domain pulse applications analysis. It enables to identify continuously the peak position from the raw pulse data and to build a histogram of the peak position for successive data records. It can also be used for ion counting or measuring the accumulated abundance of specific compounds.



AQTOF Solution Features Availability :

Table 1 presents the list of the features provided by the AQTOF solution.

	SA108	SA120	SA3xx	SA217	SA220	SA230	SA240	SA248	Comments
Digital Linearity correction			x	x	x	x	x	x	HW dependent
Calibration at Target Voltage			x			x	x	x	HW dependent
Baseline Stabilization	x	x	x	x	x	x	x	x	
Digital Equalization			x			x	x	x	Smooth, Sharp, Custom
Simultaneous Acquisition and Readout	x	x	x	x	x	x	x	x	Sustained throughput is model dependent
Real-time sampling and averaging (AVG)	x	x	x	x	x	x	x	x	
Noise Suppress Accumulation (ZS1)	x	x	x	x	x	x	x	x	
Programmable Self-Trigger	x	x	x	x	x	x	x	x	Added jitter is HW dependent
Synchronous Serial Output	x	x	x						SA1 default / SA3 Option
Peak List Mode (PKL)						x	x	x	
Partial Averaging (PKL)						x	x	x	
Observation Window (PKL)						x		x	
Peak Detection Mode (PKD)				x		x			Beta

It is important to strengthen that:

- most of features listed above may require specific HW resources to operate by themselves and may be dependent on some dedicated HW family or models.
- the simultaneous activation of some features may not be yet available or exclusive due to their current design implementation.
- the simultaneous activation of some features may limit some of the intrinsic performances of the features (e.g. trigger rate, trigger re-arm time or data readout throughput).

During consulting phase, Acqiris will advise which will be the features activated and implemented in your solution and what will be the global performance that can be expected in your application context.

Acqiris can provide on demand some specific combinations of features (e.g., AVG + PKD).

HW DAQ Modules Key specification table

SA1: 8-bits DAQ family

Table 2 presents the SA1 8-bit product family.

Key specification	SA108P	SA120P	SA108E	SA120E
Max. sampling rate	0.5 - 1GS/s	1 - 2 GS/s	0.5 - 1GS/s	1 - 2 GS/s
ADC resolution	8-bit	8-bit	8-bit	8-bit
Form factor	PCIe card	PCIe card	Serial module	Serial module
Number of channel	1	2	1	2
Bandwidth	DC - 500 MHz	DC – 500MHz	DC - 500 MHz	DC – 500MHz
Full Scale Range (FSR)	50 mV to 1V (-LVR) 250 mV to 5V (-SVR)	50 mV to 1V (-LVR) 250 mV to 5V (-SVR)	50 mV to 1V (-LVR) 250 mV to 5V (-SVR)	50 mV to 1V (-LVR) 250 mV to 5V (-SVR)
DC Offset Range	+/- 0.6 FSR/2	+/- 0.6 FSR/2	+/- 0.6 FSR/2	+/- 0.6 FSR/2
Interface	PCIe Gen 3 (Gen3 x8)	PCIe Gen 3 (Gen3 x8)	USB-C Thunderbolt 3 Serial PCIe (Gen3 x4)	USB-C Thunderbolt 3 Serial PCIe (Gen3 x4)
Data throughput	6.0 GB/s	6.0 GB/s	2 GB/s 3.0 GB/s	2 GB/s 3.0 GB/s
Power Consumption	25W	28W	30W	33W

SA2: 14-bits DAQ family

Table 3 presents the SA1 8-bit product family.

Key specification	SA217P	SA220P	SA230P	SA240P	SA248P	SA230E	SA220E
Max. sampling rate	1 - 2 GS/s	1 - 2 GS/s	4 GS/s	4 GS/s	8 GS/s	4 GS/s	2 GS/s
ADC resolution	14-bit	14-bit	14-bit	14-bit	14-bit	14-bit	14-bit
Form factor	PCIe card	PCIe card	PCIe card	PCIe card	PCIe card	Serial module	Serial module
Number of channel	1	2	1	2	1	1	2
Bandwidth	DC - 950 MHz	DC - 1.2 GHz	DC - 2 GHz	DC – 2 GHz	DC - 2.5 GHz	DC - 2 GHz	DC - 1.2 GHz
Full Scale Range (FSR)	500 mV 2.5 V (default) 1 V (-LVR)	500 mV 2.5 V	500 mV 2.5 V (default) 1 V (-LVR)	500 mV 1 V	1 V	500 mV 2.5 V 1 V (-LVR)	500 mV 2.5 V
DC Offset Range	+/- 0.6 FSR/2	+/- 0.6 FSR/2	+/- 0.6 FSR/2	+/- 0.6 FSR/2	+/- 0.6 FSR/2	+/- 0.6 FSR/2	+/- 0.6 FSR/2
Interface	PCIe Gen 3 (Gen3 x8)	PCIe Gen 3 (Gen3 x8)	PCIe Gen 3 (Gen3 x8)	PCIe Gen 3 (Gen3 x8)	PCIe Gen 3 (Gen3 x8)	USB-C Thunderbolt 3 Serial PCIe (Gen3 x4)	USB-C Thunderbolt 3 Serial PCIe (Gen3 x4)
Data throughput	6.5 GB/s	6.5 GB/s	6.5 GB/s	6.5 GB/s	6.5 GB/s	2 GB/s 3.2 GB/s	2 GB/s 3.2 GB/s

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